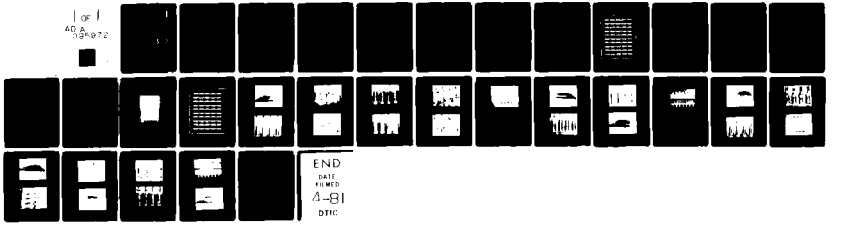
AD-A095 972 BATTELLE COLUMBUS LABS OH F/G 13/5
STANDARD SOLDER JOINT DOCUMENTATION.(U)
JAN 79 D J HAMMAN F04606-78-C-0903
UNCLASSIFIED NL



PHOTOGRAPH THIS SHEET

AD A095972

DTIC ACCESSION NUMBER

II

LEVEL

BATTELLE COLUMBUS LABS., OHIO

INVENTORY

STANDARD SOLDER JOINT DOCUMENTATION INTERIM REPT
15 Jan. 79 HAMMAN, DONALD J. CONTRACT F04606-78-C-0903

DOCUMENT IDENTIFICATION

DISTRIBUTION STATEMENT A
Approved for public release;
Distribution Unlimited

DISTRIBUTION STATEMENT

ACCESSION FOR	
NTIS	GRA&I
DTIC	TAB
UNANNOUNCED	
JUSTIFICATION	
BY Per Ltr. on file	
DISTRIBUTION / AVAILABILITY CODES	
DIST	AVAIL AND/OR SPECIAL
A	

DISTRIBUTION STAMP

DTIC
ELECTE
S MAR 5 1981 D
D

DATE ACCESSIONED

"Original contains color plates: All DTIC reproductions will be in black and white"

DATE RECEIVED IN DTIC

PHOTOGRAPH THIS SHEET AND RETURN TO DTIC-DDA-2

DTIC FORM 70A OCT 79

DOCUMENT PROCESSING SHEET

INTERIM REPORT

on

STANDARD SOLDER JOINT DOCUMENTATION

to

SACRAMENTO AIR LOGISTIC CENTER

January 15, 1979

by

Donald J. Hamman

Letter Contract No. F04606-78-C-0903

APPROVED FOR PUBLIC RELEASE - DISTRIBUTION UNLIMITED

BATTELLE
Columbus Laboratories
505 King Avenue
Columbus, Ohio 43201

TABLE OF CONTENTS

TABLE OF CONTENTS (CONT'D)

LIST OF FIGURES

LIST OF FIGURES (CONT'D)

INTERIM REPORT

on

STANDARD SOLDER JOINT DOCUMENTATION

to

SACRAMENTO AIR LOGISTIC CENTER

from

BATTELLE
Columbus Laboratories

INTRODUCTION

The Phase 1 portion of the Trend Inspection Station for Printed Circuit Board Solder Joints program is to evaluate the feasibility of using the Laser/IR, Ultrasonic and Microvideo detection techniques for detection of defective solder joints. These techniques are to be evaluated independently of each other during Phase 1. The evaluation will be based on the capability of each technique to detect specific types of solder joint defects prepared on a special printed circuit test board. The set of specific types of solder joint defects is as described in Battelle's Proposal No. 582-E-8842RR, 20 April 1978, page 24a, Auxiliary Task 1, and by Engineering Specification, Sacramento ALC, MMIRE 78-2, 2 May 1978, paragraph 3.2.1 as modified by Battelle's letter of 22 June 1978. A list of these specific defects appears later in this document.

PURPOSE

The purpose of this Interim Report is to document that the required specific solder joint defects can be and have been prepared with reasonable assurance under controlled conditions. The term "reasonable

assurance" is used because approximately one-third of the required defect types cannot be proven to exist except by destructive examination, e.g. metallographic sectioning and polishing.

DISCUSSION

The remaining portion of this Interim Report describes the types of defects prepared, the methods of preparation and provides photographic documentation of the appearance of the solder joints.

Types of Defects

The following types of solder joints were required to be prepared according to the proposal, specification and letter cited in the Introduction. The letter designations associated with the defects listed below are the same as those in the Sacramento ALC specification except that Battelle has added the "t" and "z" designations. Defect h was deleted because it was redundant with i, n_1 and q. Defect m was not produced because the formation is a long term process and our acceleration techniques were unsuccessful.

a. Cold solder joint.
b. Irregular spreading of solder up lead due to excessive heat applied during soldering.
c. Irregular spreading of solder up lead due to insufficient heat applied during soldering.
d. "Toe" of lead bent up.
e. Lead soldered 1/2 off pad.
f. Tipped lead.
g. Yellow flat top of lead viewed.
h. ~~Lead pressed down too hard during soldering resulting in solder being squeezed out and a void in the middle area under the lead~~. DELETED
i. Voids in solder.
j. Cracks at heel of joint.
k. Granular appearance.
l. $AuSn_4$ and $AuSn_2$ entrapped in solder joint microstructure.
m. Copper Abietate (green).

n_1. Insufficient solder.
n_2. Excess solder.
o. Excessive heat.
p. No fillet at heel/lead.
q. Dewetted joint.
r. Holes and pits.
s. Solder peaks.
t. Inclusions.
z. Good joint.

These joint types were prepared using gold coated, 14-lead flat pack style integrated circuit packages and a printed circuit board (PCB) with a layout as shown in Figure 1.

Equipment Used

All solder joints were formed using a Hughes Microgap Welder, Model MCW-550 incorporating a Model VTA-60 attachment with a spacing of 0.040 inbetween the parallel tips. This equipment permits a wide range of pulse voltages and pulse durations.

Solder Joint Procedures

The descriptions that follow summarize the methods and conditions used to prepare the specific types of solder joints required for this Phase 1 program. All joints were made using solder tinned leads on the flat packs and solder coated pads on the PCB. The only exception ot the lead tinning was in the preparation of "g", yellow flat top of lead viewed. In this case, the top of the lead was masked prior to tinning so that no tinning of the lead top occurred.

The details of determining the procedures and conditions are contained in Battelle's Laboratory Record Book No. 34373.

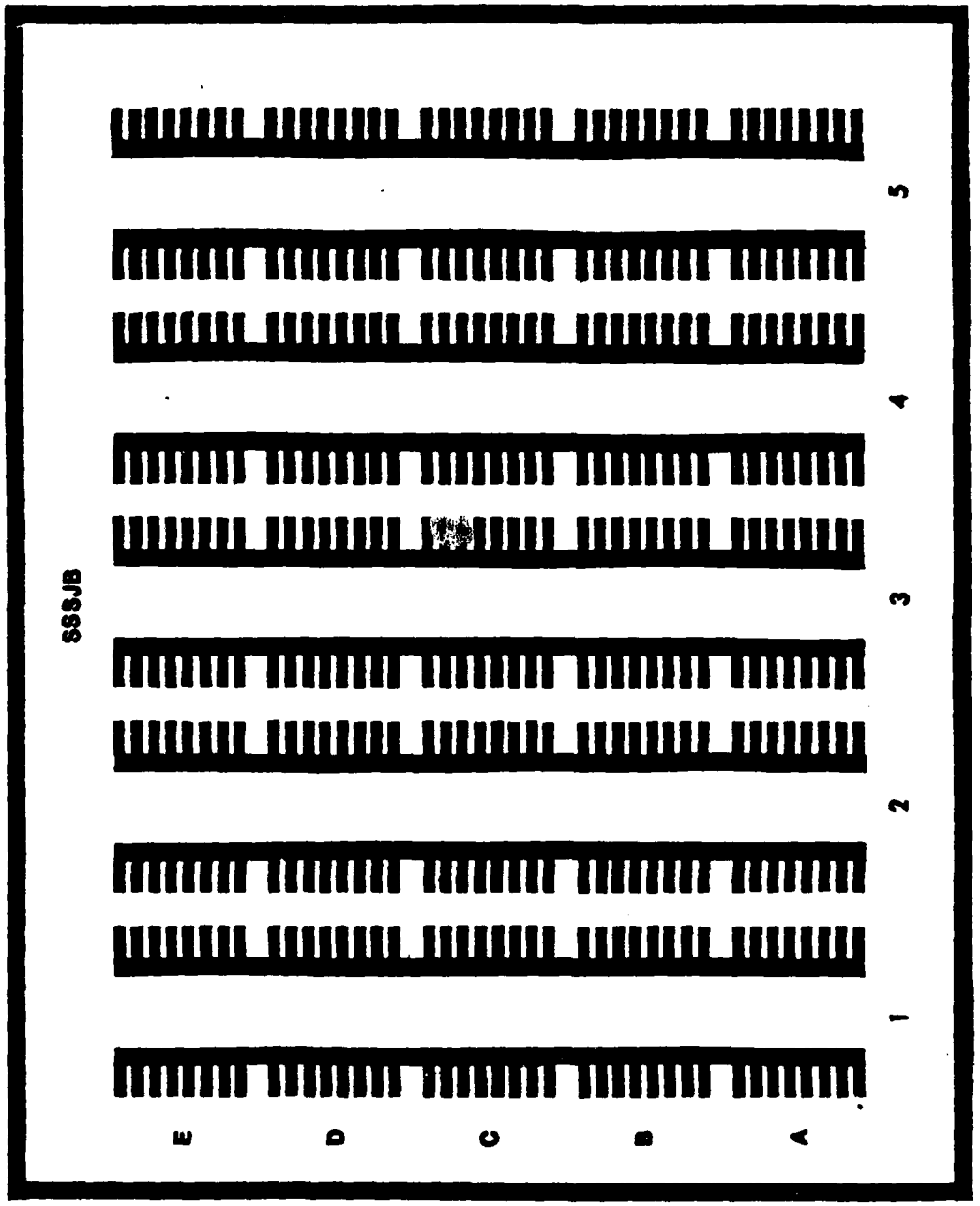


FIGURE 1. PRINTED CIRCUIT BOARD LAYOUT FOR STANDARD SOLDER JOINTS

Good Joint (z)

The conditions necessary to produce consistently good solder joints were developed first. This development consisted of determining the necessary power conditions, the tinning requirements for both the leads and pads and the amount of solder required. Essentially this same procedure was followed for each joint type with appropriate modifications.

The power pulse conditions for good joints were determined to be 0.32 volt (V) for 0.130 second(s).

Cold Solder Joint (a)

The power pulse conditions were 0.32 V for 0.210 s. The reason for the longer pulse is as follows. The Hughes Microgap Welder operates normally by:

(1) Bringing the welding tips into contact with the lead,
(2) Pressing the lead against the PCB pad,
(3) Applying the power pulse to the tips (thus heating the solder and allowing it to reflow),
(4) Permitting the solder to refreeze,
(5) Releasing the welding tips.

However, in the case of the cold solder joints, the tip pressure is released before the solder refreezes. The inherent springiness of the lead material allows the lead to move while the solder refreezes. This motion during refreezing results in a cold solder joint.

Irregular Spreading Due to Excessive Heating (b)

Power pulse conditions were 0.32 V for 0.260 s.

Irregular Spreading Due to Insufficient Heating (c)

Power pulse was 0.32 V for 0.090 s.

Toe of Lead Bent Up (d)

Power pulse was 0.32 V for 0.130 s. The tip of the lead was mechanically bent up before soldering.

Lead Soldered One-Half Off Pad (e)

Power pulse was 0.32 V for 0.130 s. The lead was mechanically displaced before soldering.

Tipped Lead (f)

Power pulse was 0.32 V for 0.130 s. The lead was mechanically twisted before soldering.

Yellow Flat Top of Lead Viewed (g)

Power pulse was 0.32 V for 0.130 s. In addition, the top of the gold plated lead was masked prior to tinning so that the top of the lead remained untinned, thus leaving exposed gold after soldering.

Voids In Solder (i)

Power pulse was 0.32 V for 0.160 s. The voids were produced by scribing a small trench (approximately 0.030 in by 0.010 in) in the solder coating of the PCB pad. A small quantity of Polyox WSR-35 was placed in the trench. The joint was then soldered using the normal procedure. During the heating pulse, the Polyox was volatilized thus producing a void space between the lead and the PCB pad.

Cracks at Heel of Joint (j)

Power pulse was 0.32 V for 0.130 s. The heel of the joint was stressed after the solder joint was made to induce a crack at the heel.

Granular Appearance (k)

Power pulse was 0.32 V for 0.130 s. The granular appearance of these joints was produced by introducing a small amount of Wood's Metal into the solder joint. Wood's Metal is a low melting point (70 C) alloy consisting of 50 percent bismuth, 25 percent lead and 12.5 percent each of tin and cadmium.

$AuSn_4$ and/or $AuSn_2$ Entrapped In Solder Joint Microstructure (l)

Power pulse was 0.32 V for 0.180 s. This joint type was produced by introducing a small amount of gold into the solder joint to form a gold-enriched joint. The availability of the excess gold coupled with the pulse heating of the joint produces the desired gold-tin compounds.

Copper Abietate (Green) (m)

This defect was not produced. The formation of copper abietate requires the presence of exposed contaminated copper, the use of a flux containing abietic acid, incomplete cleaning of the flux residue and extended time. Our attempts to accelerate the formation process were unsuccessful.

Insufficient Solder (n_1)

Power pulse was 0.32 V for 0.130 s. The solder was removed (except for a thin tinning film) from the PCB pad prior to making the solder joint.

Excess Solder (n_2)

Power pulse was 0.32 V for 0.130 s. Extra solder was added to the PCB pad prior to making the solder joint.

Excessive Heat (o)

Power pulse was 0.42 V for 0.130 s. The higher voltage resulted in excess heating to the lead and PCB pad. It must be noted that the increase from 0.32 V to 0.42 V is sufficient to cause some color change in the PCB substrate. There is also some evidence of a slight tendency for the copper to delaminate from the PCB substrate.

No Fillet at Heel of Lead (p)

Power pulse was 0.32 V for 0.130 s. The lack of fillet was produced by controlling the amount of solder available at the heel of the joint.

Dewetted Joint (q)

Power pulse was 0.32 V for 0.130 s. In addition, the solder tinning was removed from the PCB pad prior to making the solder joint, and the bottom of the flat-pack lead was untinned. Strictly, this is an unwetted joint. However, the appearance and effect are the same as dewetted.

Holes and Pits (r)

Power pulse was 0.32 V for 0.160 s. The solder tinning on the PCB pad was perforated in several places, and the perforations were filled with Polyox WSR-35. When the solder joint was made, the heat volatilized the Polyox and the escaping gas formed holes and/or pits in the solder.

Solder Peaks (s)

Power pulse was 0.132 V for 0.130 s. The solder peaks were produced by touching the completed solder joint with a hot, solder-wettable soldering tip. The action of withdrawing the tip left a solder peak.

Inclusions (t)

Power pulse was 0.32 V for 0.160 s. The inclusions were produced by forming a trench in the PCB pad solder coat as in Voids (i) and filling the trench with powdered graphite prior to making the solder joint.

PICTORIAL DOCUMENTATION

This portion of the Interim Report presents the pictorial documentation demonstrating the ability to form the required solder joint types using the conditions and methods summarized above. Figure 2 is a photograph of the overall PCB containing the 20, flat-pack integrated circuit packages. The defect types and locations are shown in the defect map of Figure 3. The black dot in Figures 2 and 3 represents the location of pin number 1 of the flat pack.

Figures 4 through 29 are photographs of the solder joint types prepared for the "standard" solder joint set shown in Figure 2. In general, the captions with the photographs are self-explanatory. However, additional explanation has been added where necessary.

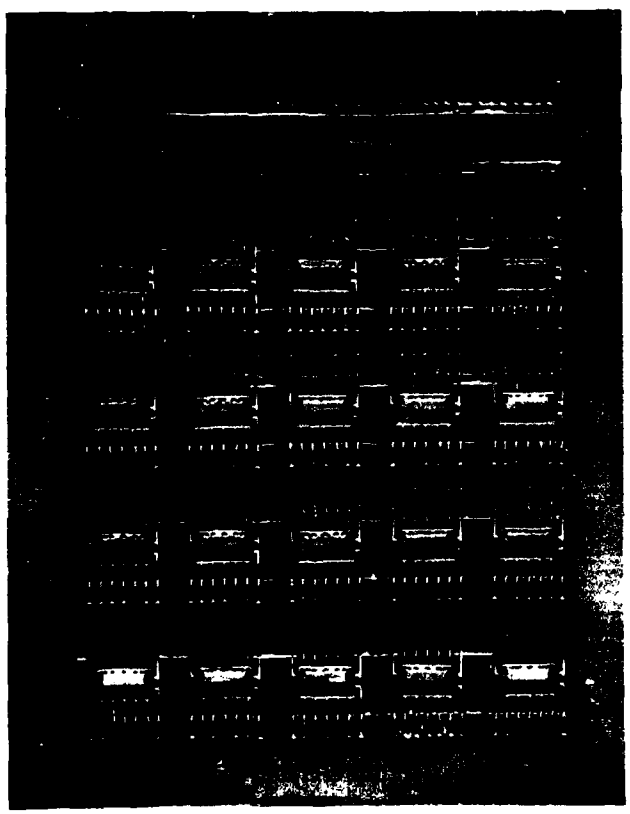


FIGURE 2. OVERALL PHOTOGRAPH OF PCB WITH MOUNTED 1C FLAT PACKS

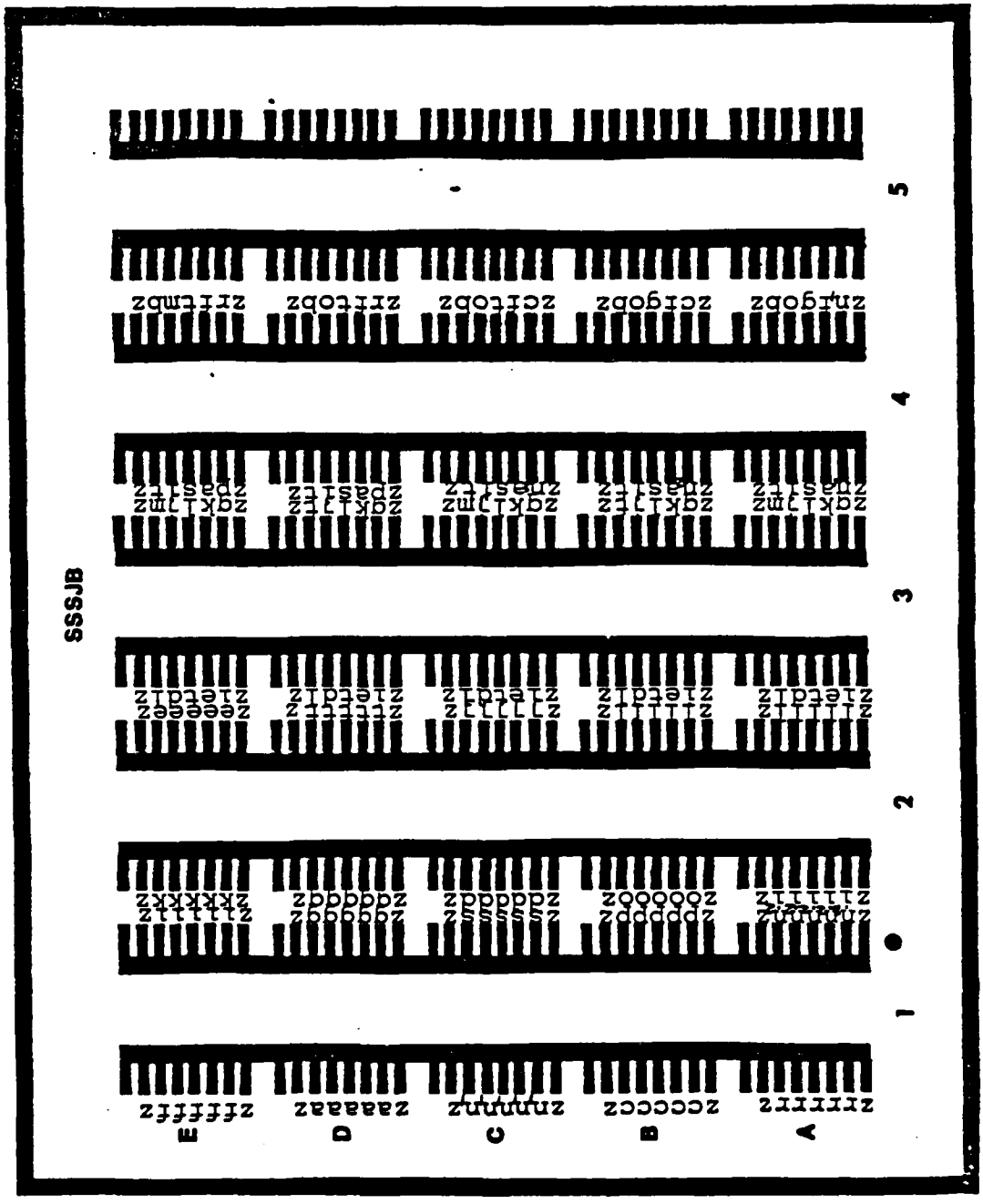


FIGURE 3. DEFECT MAP

FIGURE 4. GOOD SOLDER JOINT (z)

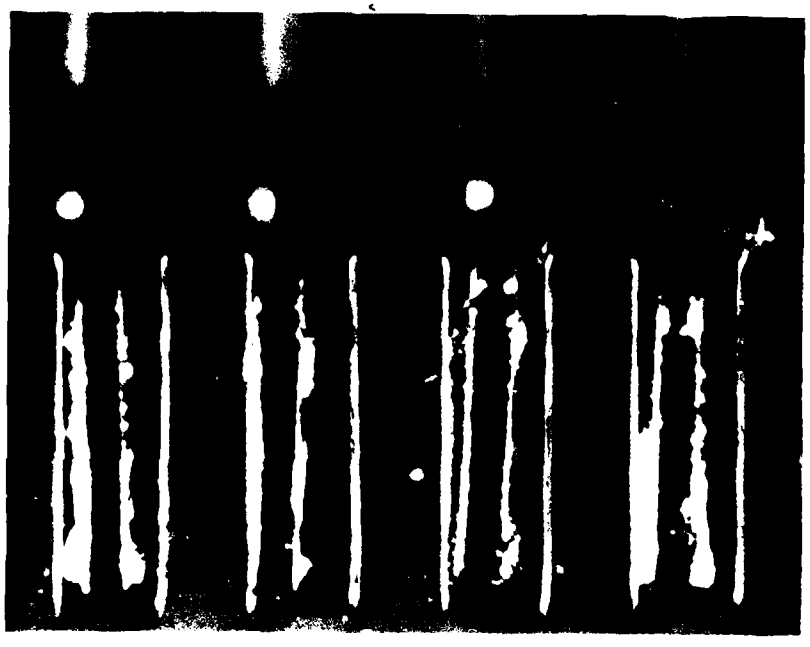


FIGURE 5. COLD SOLDER JOINTS (a)

FIGURE 6. IRREGULAR SPREADING-EXCESSIVE HEAT (b)

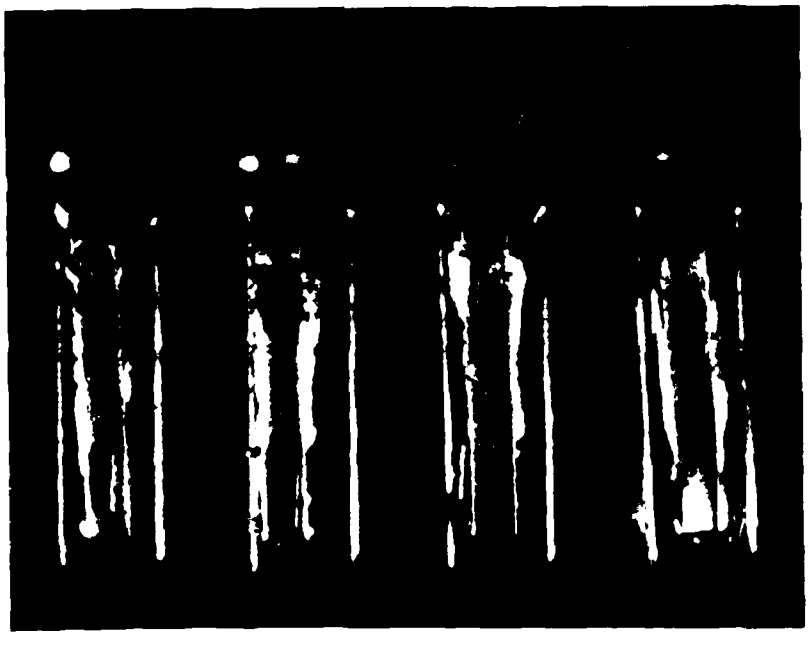


FIGURE 7. IRREGULAR SPREADING-INSUFFICIENT HEAT (c)

FIGURE 8. TOE OF LEAD BENT UP (d)

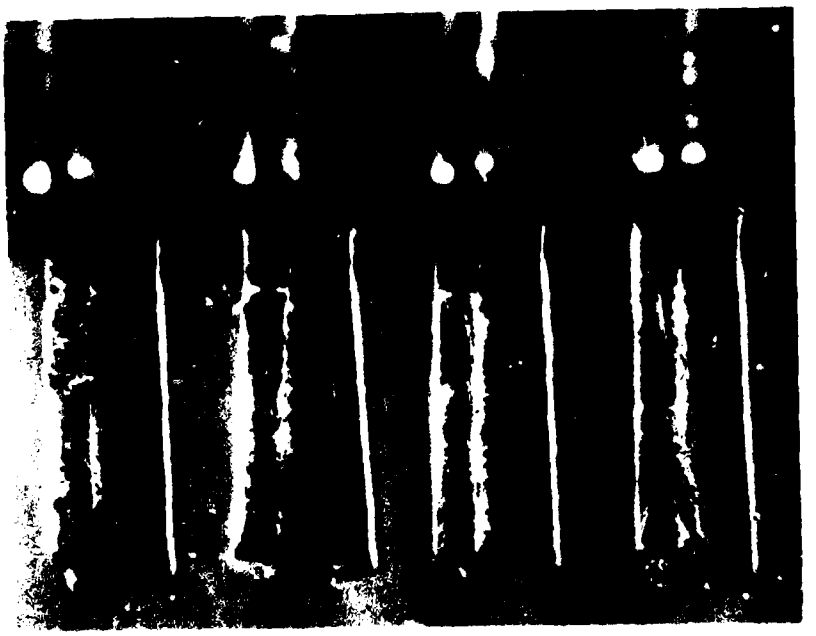


FIGURE 9. LEAD HALF OFF PAD (e)

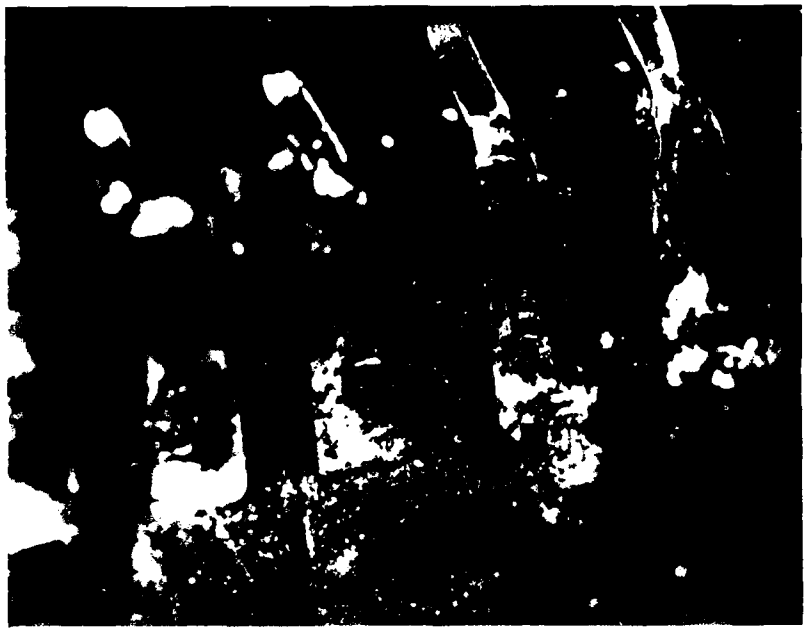


FIGURE 10. TIPPED LEADS (f)

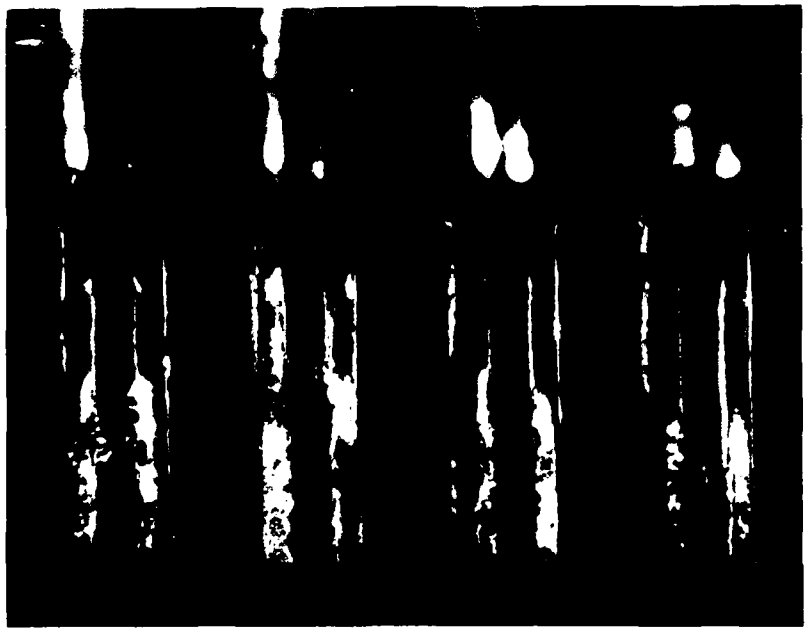


FIGURE 11. YELLOW TOP OF LEAD-EXPOSED GOLD (g)

FIGURE 12. VOIDS IN SOLDER JOINT (i)

Figure 12 is a metallographic section through a set of 14 solder joints all on the same 1C flat pack. The black dot in the upper left hand corner designates lead number 1. The leads are numbered clockwise with number 14 directly below number 1. Leads numbered 1, 7, 8 and 14 are good joints. All others contain voids between the lead and the PCB pad.

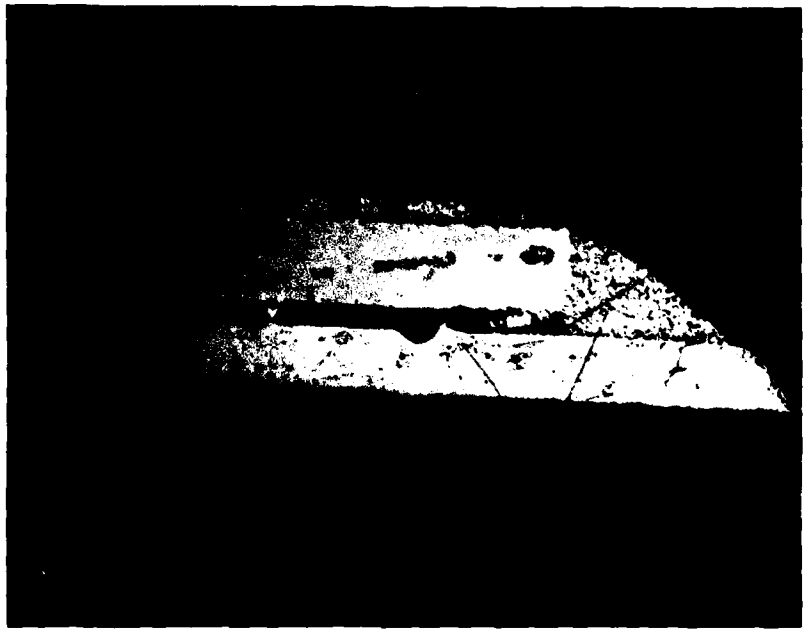


FIGURE 13. VOID UNDER LEAD (i)
(Pin No. 2 of Figure 12)

FIGURE 14. CRACKS AT HEEL (j)

FIGURE 15. GRANULAR APPEARANCE (k)

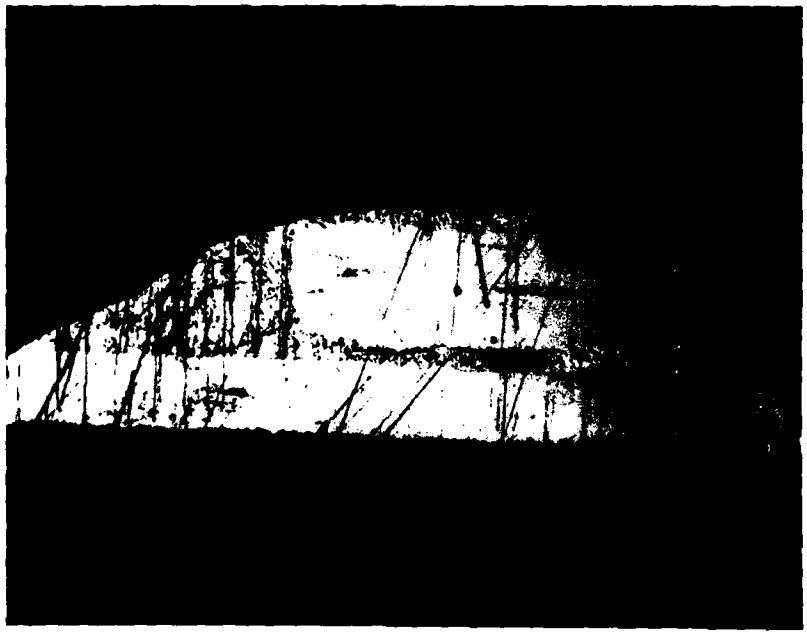


FIGURE 16. SECTION THROUGH GRANULAR JOINT (k)
(Pin No. 12 of Figure 15. Note internal similarity to good joint.)

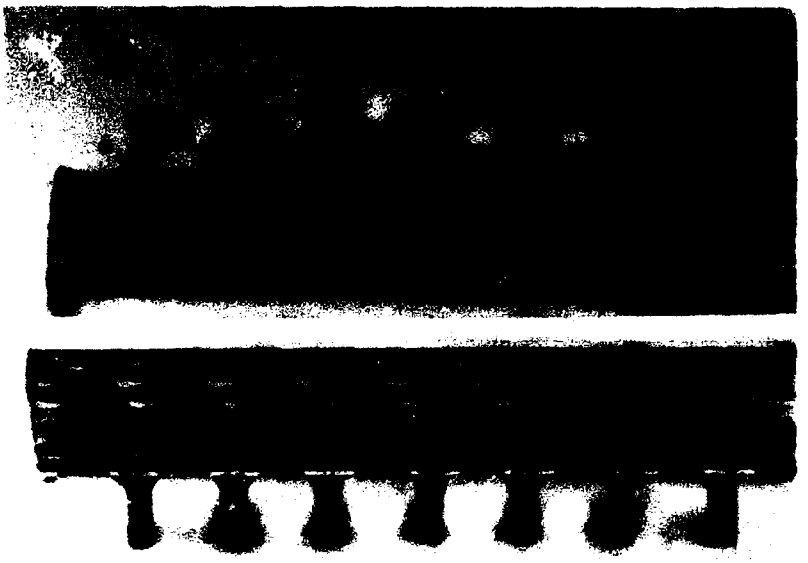


FIGURE 17. $AUSN_4$ AND $AUSN_2$ IN JOINT (1)

The black dot is lead number 1 and numbering continues clockwise. Again leads 1, 7, 8 and 14 are normal joints. The other 10 joints are all gold enriched. The photograph is not intended to show detail (see Figure 18), but is only to demonstrate that the joint type can be made consistently.

FIGURE 18. GOLD ENRICHED JOINT (1)

The $AuSn_4$ and $AuSn_2$ intermetallics appear at the interface between the gold and solder. This joint was chosen to exaggerate the presence of gold for easy visibility.

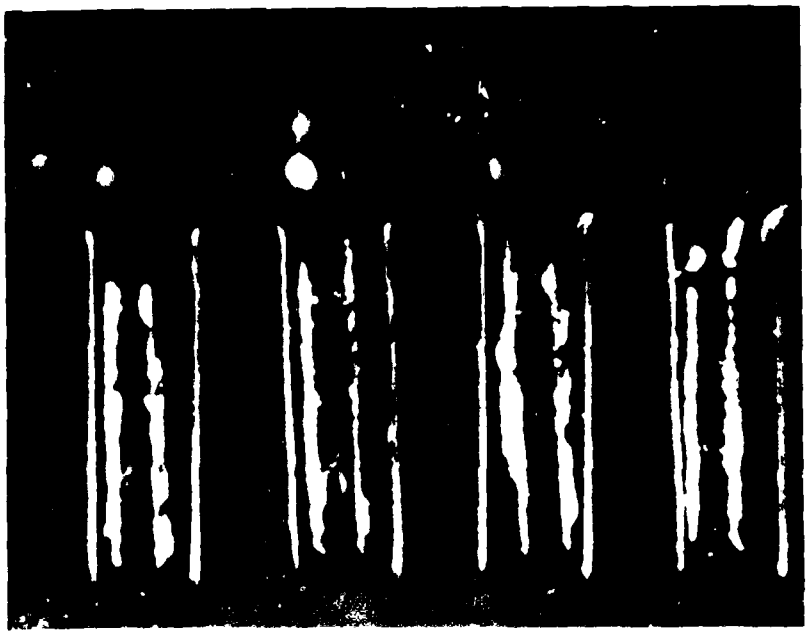


FIGURE 19. INSUFFICIENT SOLDER (n_1)

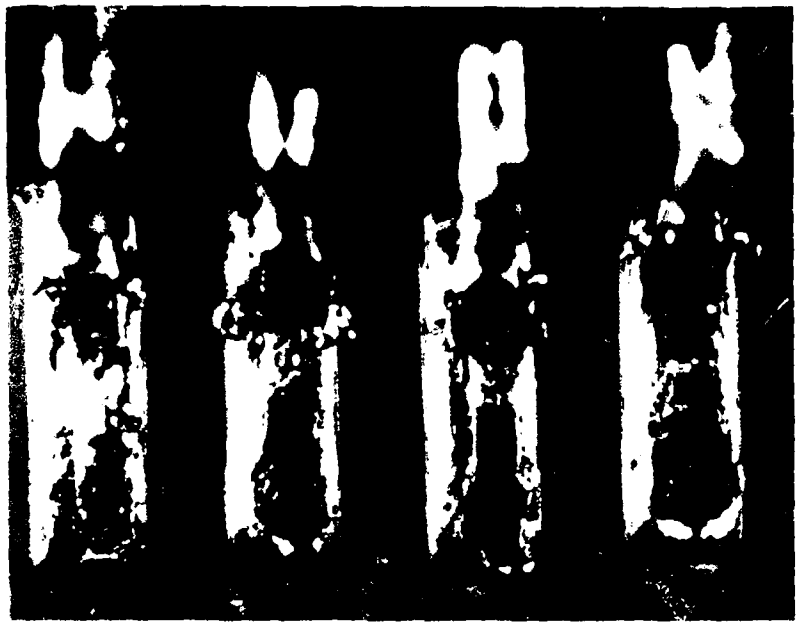


FIGURE 20. EXCESS SOLDER (n_2)

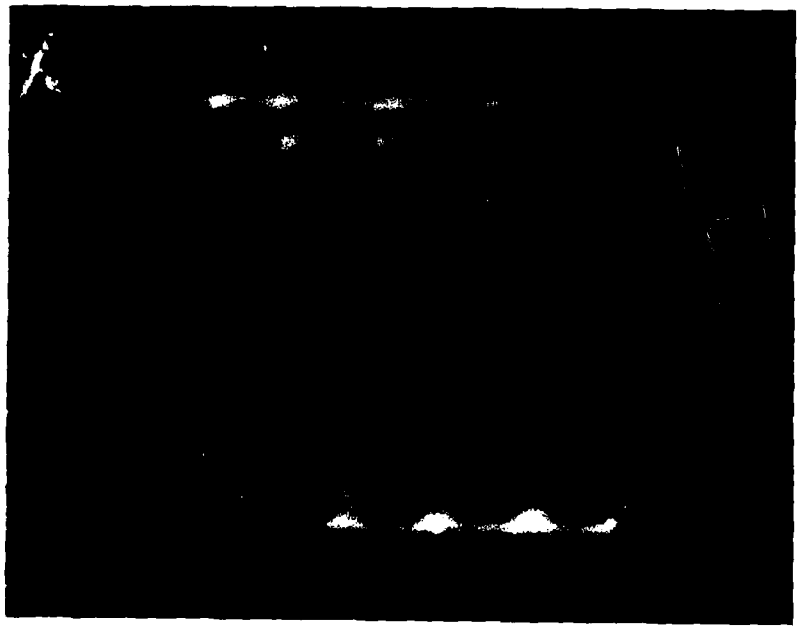


FIGURE 21. EXCESSIVE HEAT (o)

Only the joint at lead number 5 (arrow) was subjected to excessive heat. Note deformation of substrate.

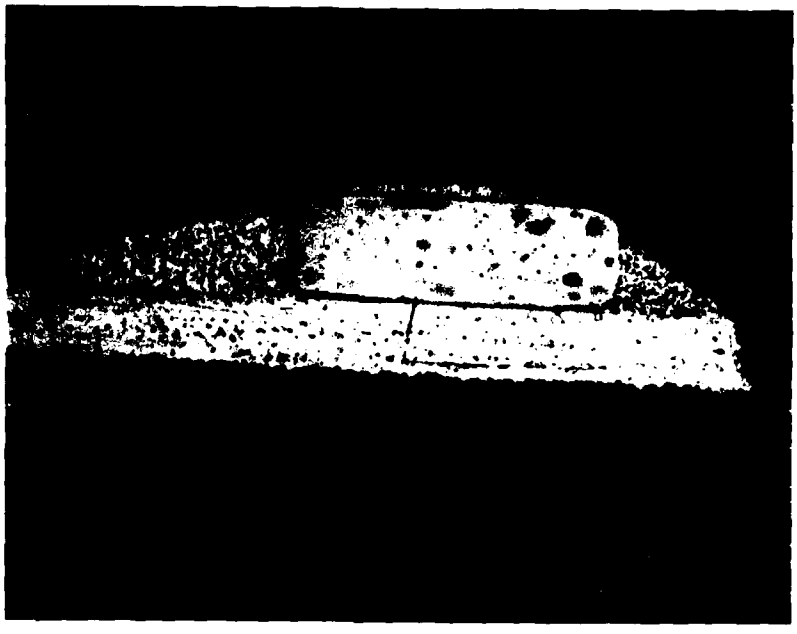


FIGURE 22. EXCESSIVE HEAT (o)

Lead number 5 of Figure 21. Note "spongy" appearance of solder as compared to good joint of Figure 4.

FIGURE 23. NO SOLDER FILLET AT HEEL (p)

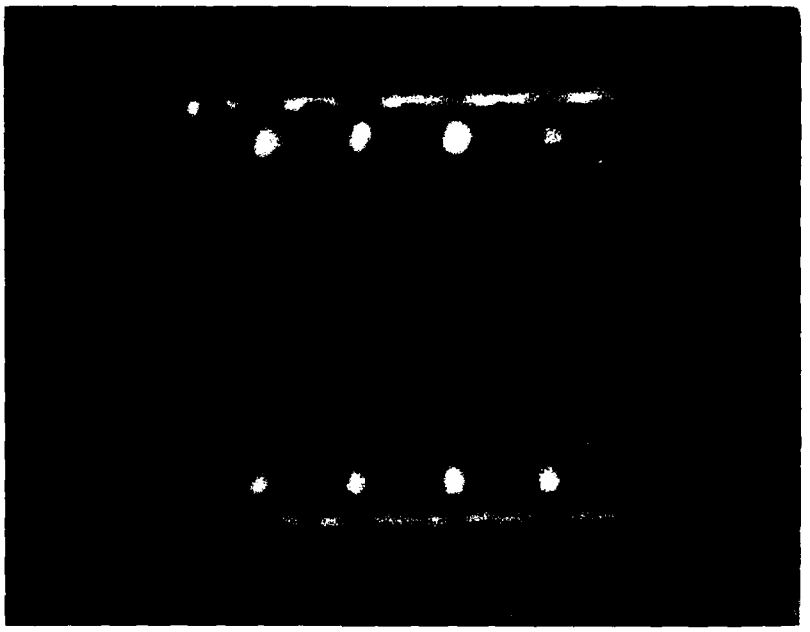


FIGURE 24. DEWETTED JOINT (q)

At arrow and see Figure 25.

FIGURE 25. DEWETTED JOINT (q)

Lead number 11 of Figure 24.

FIGURE 26. HOLES AND PITS IN SOLDER (r)

FIGURE 27. SOLDER PEAKS (s)

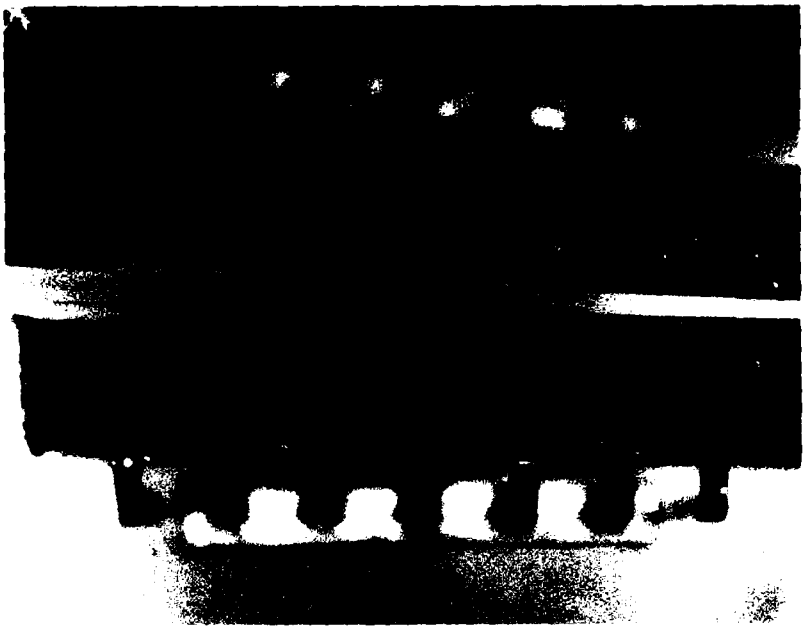


FIGURE 28. FOREIGN INCLUSIONS (t)

Inclusions under leads 2 through 6
9 through 13

FIGURE 29. POWDERED GRAPHITE INCLUSION UNDER LEAD

Number 11 of Figure 28.

SUMMARY AND CONCLUSION

It is always the intent, when making solder joints for electronics, that the completed joint be electrically continuous and mechanically strong. A joint that is defective is always the result of defective materials, improper techniques or poor workmanship. However, the intent of this Auxiliary Task was to produce known types of defects, not once, but consistently. This required the development of various techniques that were summarized earlier in this report.

Some of the defect types were quite easy to produce, such as those requiring only mechanical displacement or distortion, (d, e, f, j, n_1, n_2, p, q, s). Others such as those requiring excessive or insufficient heat (b, c, o) were a little more difficult in that the power pulse deviations from nominal lead need to be determined. Still others, particularly those involving voids, holes and pits, foreign inclusions, granular appearance, cold joints and gold-tin compounds (a, g, i, k, l, r, t) were extremely difficult problems to produce consistently. These required the identification of special materials (suitable contaminants), deviant power pulse conditions and/or unusual mechanical techniques.

This Auxiliary Task was considerably more difficult and entailed much more effort than expected at the beginning of the program. However, we believe the resulting sets of "calibrated" or "standard" solder joint defects will be satisfactory for the needs of the program.

The resulting sets of "standard" joints have been sent to Dr. Traub at Vanzetti for the Laser/IR study and to D. Ensminger at Battelle for the ultrasonic study.


DAT
FILM
4